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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,786	01/21/2004	Theodore C. White	MP0795	3539

26703 7590 02/21/2007

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EXAMINER	
SUN, SCOTT C	
ART UNIT	**PAPER NUMBER**
2182	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/761,786	WHITE ET AL.	
	Examiner	Art Unit	
	Scott Sun	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1/5/2007 has been entered.

Response to Arguments

2. Applicant's arguments filed 1/5/2007 have been fully considered but they are not persuasive. Applicant's arguments are summarized as:

a. Prior art of record does not teach "a read assembly module... that extracts the first and second data segments from the read plurality of data blocks based on the data lengths and data start addresses" (emphasis added).

3. In response to argument 'a', examiner notes that applicant argues that prior art of record, *Budd*, does not disclose storing "data lengths of first and second data segments" but instead teaches storing "a size of the buffer portion identified by the address" (emphasis added). Examiner asserts that the "size of the buffer portion identified by the address" taught by *Budd* is equivalent to the length of the segments in applicant's disclosure. In *Budd*'s disclosure, the size and address fields shown in figure 20 and the cited paragraph are part of a scatter-gather data structure (column 23, lines 23-37), which is used to regroup fragments of data created by write operations during a read

operation – hence scatter-gather (column 14, lines 3-14). To identify each of the data fragments, each entry in the scatter-gather list includes two fields; namely the address and the size of the buffer space in which the fragments are stored. The address identifies the starting location of a particular fragment stored in memory, while the size of the buffer portion indicates the size of the data fragment identified by the address, as Budd clearly states that "using this particular data structure, the actual physical location of data or memory locations associated with a logical data buffer may be represented" (emphasis added).

As a further note, examiner points to paragraph 34 of applicant's disclosure. In the disclosure, applicant also uses scatter-gather entries to describe the data segments. The difference between applicant's disclosure and Budd's is the size of the data segments are called "length" instead of "size", but as stated above, these entries are no different in functionality.

4. Having responded to each of applicant's arguments, examiner notes that prior art of record still provides a valid ground of rejection. Minor changes are made to reflect the amended claims.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 14-16, 18, 19, 24-26, 28, 29, 33-35, 37, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aruga (US 2003/0097525) in view of Budd et al (US Patent # 7,003,702).

7. Regarding claims 14, Aruga discloses a storage controller (disk array controller 1, figure 2), comprising: a read assembly module (parity generator 9 and host and disk interface controllers), that receives a request to read the first and second data segments from a host, that reads the plurality of data blocks (data blocks and parity data blocks) from the first memory, extracts (concatenate) the first and second data segments from the read plurality of data blocks, and that transfers the first and second data segments contiguously to the host (paragraphs 27, 28). Examiner notes that Aruga teaches when transferring data to the host, data segments are concatenated in the parity data generator and subsequently transferred to the host. Furthermore, the data need to be stored in the storage controller during the processing, and therefore the storage controller contains a first memory that stores the plurality of blocks that include first and second noncontiguous data segments.

Aruga does not teach a queue module that stores data lengths and data start addresses of the first and second data segments or extracting based on the data lengths and data start addresses. However, Budd teaches a queue module (scatter-gather list) that stores data lengths (size field 902b) and data start addresses (ptr field 902a) of the first and second data segments, and extracts the first and second data segments from the read plurality of data blocks based on the data lengths and data start addresses (function of the scatter-gather list; column 23, lines 23-37). Teachings of

Aruga and Budd are from the same field of storage systems, and specifically of transferring data from disk storage to host.

Therefore, it would have been obvious at the time of invention for a person of ordinary skill in the art to implement a scatter-gather list in the system of Aruga for the benefit of easily mapping fragmented physical locations to contiguous logical locations. Examiner further notes that such information (address and length of data) would also be needed for the concatenation of the data segments as disclosed by Aruga.

8. Regarding claims 15, Aruga and Budd combined disclose claim 14, and Aruga further discloses wherein the read plurality of data blocks include data integrity data (parity data, paragraph 27). Examiner notes that parity data is generated for storing with the raw data, which is later used to check for error detection when retrieving data from disk.

9. Regarding claim 16, Aruga and Budd combined disclose claim 15 but do not disclose explicitly using CRC as the type of integrity verification data. However, examiner notes that CRC is a widely known type of error correction/detection method at the time of invention. Given the teachings of Aruga to use integrity data, it would have been obvious for one of ordinary skill in the art at the time of invention to implement CRC as the type of integrity data because they are simple to implement in binary hardware, are easy to analyze mathematically, and are particularly good at detecting common errors.

10. Regarding claim 18, Aruga and Budd combined disclose claim 14, and Aruga further discloses wherein the read assembly module concatenates the first and second data segments (paragraph 28).

11. Regarding claim 19, Aruga and Budd combined disclose claim 14, and Aruga further discloses a second memory (cache memory 8), wherein the read assembly module transfers the first and second data segments to the second memory and the second memory transfers the first and second data segments to the host (paragraph 28).

12. Claims 24-26, 28, 29, 33-35, 37, 38 are substantially similar to claims 14-16, 18, 19 above. They are rejected using the same arguments. Examiner notes that the storage device in teachings of Aruga and Budd are disk drives.

13. Claims 17, 27, 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aruga in view of Budd, and further in view of Wyatt et al (PG Pub# 2003/0172325).

14. Regarding claim 17, Aruga, and Budd combined disclose claim 15 but does not disclose explicitly not transferring data integrity verification data to the host. However, Wyatt teaches that data integrity verification data (parity data) is removed and not sent to the host (paragraph 10). Teachings of Wyatt, Aruga, and Budd are from the same field of storage devices, and specifically of transferring data from device to host.

Therefore, it would have been obvious at the time of invention to combine teachings of Aruga, Budd, and further with teachings of Wyatt by deleting integrity

verification data before sending data to the host for the benefit of efficient bandwidth use.

15. Claims 27 and 36 are substantially similar to claim 17 above. They are rejected using the same arguments.

16. Claims 21-23, 31, 32, 40, 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aruga (US 2003/0097525) in view of Budd et al (US Patent # 7,003,702) and further in view of applicant's admitted prior art.

17. Regarding claim 21, Aruga, and Budd combined disclose claim 14, but does not disclose explicitly the first memory is a buffer memory. However, applicant's admitted prior art further discloses wherein the first memory is a buffer memory. Teachings of Aruga, Budd, and applicant's admitted prior art are from the same field of storage systems, and specifically of transferring data from disk storage to host.

Therefore, it would have been obvious at the time of invention to combine teachings of Aruga and Budd, and further with teachings of applicant's admitted prior art by using a buffer as memory to hold data segments for the benefit of temporarily storing data being transferred to compensate for speed differences between host and disk storage.

18. Regarding claim 22, Aruga, Budd, and applicant's admitted prior art combined disclose claim 14, and applicant's admitted prior art further discloses wherein the buffer memory receives the first and second data segments from a storage device (paragraph 5, 6).

19. Regarding claim 23, Aruga, Budd, and applicant's admitted prior art combined disclose claim 14, and Aruga further discloses wherein the storage device is a hard disk drive (figure 1).

20. Claims 31, 32, 40, 41 are substantially similar to claim 20 above. They are rejected using the same arguments.

21. Claims 20, 30, 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aruga in view of Budd and applicant's admitted prior art, and further in view of Proch et al (PG Pub 2001/0054121).

22. Regarding claim 20, Aruga and Budd combined disclose claim 15 but does not disclose the second memory is a FIFO buffer. However, Proch teaches that FIFOs are used for data transfers from disk drive to host and vice versa (paragraphs 8-11). Teachings of Proch, Aruga, and Budd are from the same field of storage devices, and specifically of transferring data from device to host.

Therefore, it would have been obvious at the time of invention to combine teachings of Aruga, Budd, and further with teachings of Proch by storing the data in a FIFO buffer before sending to the host for the benefit transfer speed synchronization between host and storage device.

23. Claims 30 and 39 are substantially similar to claim 20 above. They are rejected using the same arguments.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Sun whose telephone number is (571) 272-2675. The examiner can normally be reached on M-F, 10:30am-7pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

KIM HUYNH
SUPERVISORY PATENT EXAMINER
2/17/07